What is claimed is:

1. A semiconductor device comprising:

a plurality of ferroelectric capacitors for memory in which each one end thereof is connected to each of a plurality of first bit lines via switching transistor;

first plate lines connected to the other ends of said ferroelectric capacitors for memory;

first ferroelectric capacitors for reference in which each one end thereof is connected to a second bit line via first n-channel MOS transistor;

a second plate line connected to the other ends of said first ferroelectric capacitors for reference; and

a p-channel MOS transistor connected to said second plate line.

2. A semiconductor device according to claim 1, wherein said p-channel MOS transistor is formed in a plate driver circuit to which said first plate lines and said second plate line are connected.

3. A semiconductor device according to claim 2, wherein said plate driver circuit has a structure that the circuit applies voltage lower than that of said second bit line to said second plate line via said p-channel MOS transistor in an ON state of said p-channel MOS transistor.

4. A semiconductor device according to claim 1, wherein said switching transistor is n-channel MOS transistor.

5. A semiconductor device according to claim 1 further comprising:

a sense amplifier that amplifies voltage variation quantity of said first bit lines and voltage variation quantity of said second bit line.

6. A semiconductor device according to claim 1 further comprising:

second ferroelectric capacitors for reference in which each one end thereof is connected to a third bit line via second n-channel MOS transistor;

a third plate line connected to the other ends of said ferroelectric capacitors for reference; and

a third n-channel MOS transistor connected to said third plate line.

7. A semiconductor device according to claim 6, wherein the number of said first ferroelectric capacitors for reference is 1% or less of a total number of said second ferroelectric capacitors for reference and said first ferroelectric capacitors for reference.

8. A semiconductor device according to claim 1, wherein said first ferroelectric capacitors are elements to which data having minus polarization charge is written before heat treatment.

9. A semiconductor device according to claim 8, wherein said heat treatment is performed at 200°C or more.

10. A semiconductor device comprising:

a memory cell region of 2T2C type, which stores 1-

bit by first and second transistors and first and second ferroelectric capacitors for memory; and

a memory cell region of 1T1C type, which stores 1-bit by a third transistor and a third ferroelectric capacitor for memory.

11. A semiconductor device according to claim 10, wherein said memory cell region of 2T2C type is a region corresponding to a range having 1% or less of the number of said bits.

12. A semiconductor device according to claim 10, wherein said memory cell region of 2T2C type is a region to which data is written before heat treatment.

13. A semiconductor device according to claim 12, wherein said heat treatment is performed at 200°C or more.